

MSP8520

Multi-Service Security Processor

Released
Product Brief

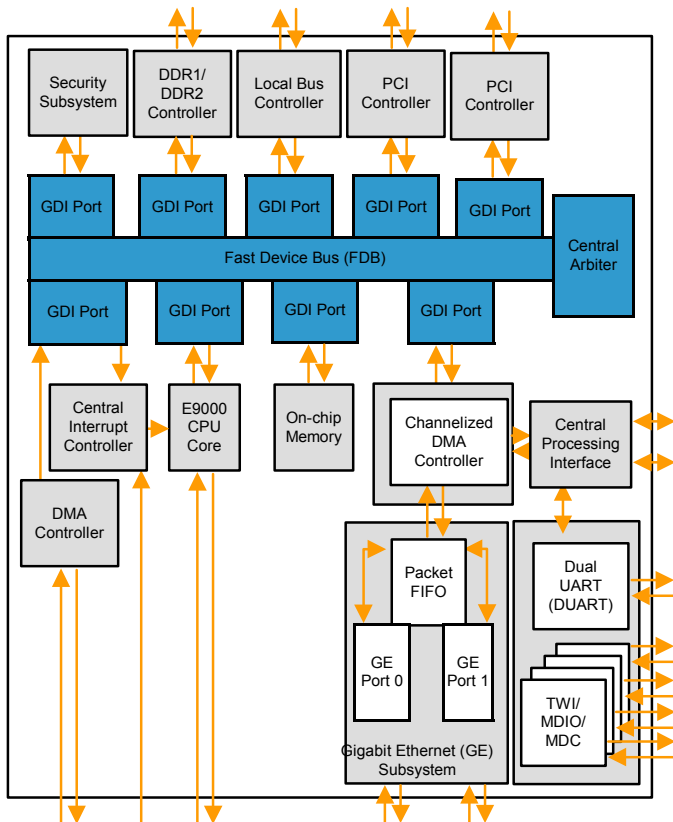
PRODUCT OVERVIEW

PMC-Sierra's MSP8520 Multi-Service Security-enabled processor is designed to meet the needs of IP storage, networking, security appliances, and office automation.

MSP8520 device integrates standards-based hardware security to accelerate internet protocol security (IPSEC) and secure socket layer (SSL) performance for security appliances, firewalls, networking, IP storage and laser printers/MFPs.

The MSP8520 is part of the MSP8500 Series of highly-integrated, feature-rich products that incorporate PMC-Sierra's high performance E9000 microprocessor core. The MSP8520 uses the high-bandwidth Fast Device Bus (FDB) as the system bus to interconnect all the on-chip devices to each other and to the E9000 microprocessor using the Generic Device Interface (GDI). All MSP8500 Series products provide a variety of interfaces including PCI, Ethernet, and ROM, Flash, Compact Flash, SRAM, and other low-speed peripheral interfaces.

BLOCK DIAGRAM

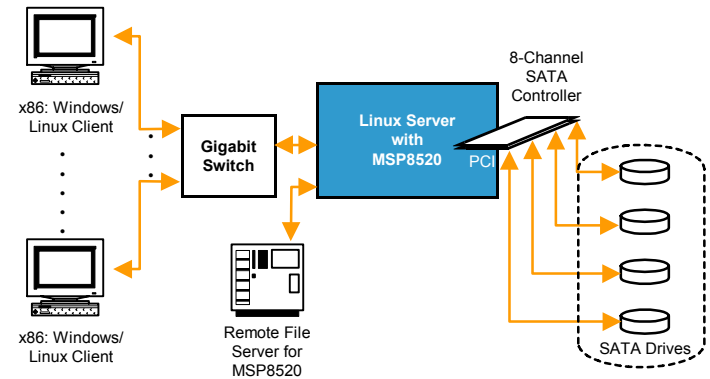


PRODUCT HIGHLIGHTS

- Integrated Security subsystem:
 - Dedicated 4-channel DMA controller for security packet processing
 - IPsec engine:
 - Supports all IPsec packet transforms and implements SSL packet transforms
 - Implements DES/3DES/AES/RC4 crypto and SHA-1/MD-5 hash algorithm support
 - Random number generator
 - Public key accelerator
- E9000 microprocessor core:
 - 600 MHz to 1 GHz operation
 - Dual-issue superscalar 7-stage pipeline
 - 16 Kbyte L1 Instruction and Data caches with parity and a 256 Kbyte L2 cache with ECC support
 - 8K entry branch prediction table
 - Multiple reads with out-of-order return
 - MMU with 128 total TLB entries, page size range: 4 Kbytes to 256 Mbytes
 - High-performance Floating Point Unit (IEEE 754)
 - Fixed-point DSP instructions
- 400 MHz Fast Device Bus (FDB) system interconnect:
 - Multiple master, shared, on-chip bus
 - Bus performance monitoring
 - Connects the E9000 CPU and other peripherals to memory and I/O interfaces
- 167 – 200 MHz DDR1/DDR2 SDRAM memory controller with a 64-bit data interface:
 - Supports Class I and Class II SSTL drive strengths
 - Supports maximum addressing up to 4 Gbytes
 - Provides DDR2 single-ended DQS signaling so that DDR2 RAMs may be supported and operated in DDR1 mode
 - DDR1 supports device densities of 64, 128, 256, 512 Mbits and 1 Gbit, DDR2 supports densities of 256, 512 Mbits and 1 Gbit
 - DDR2 supports device widths of 8 and 16 bits. DDR1 additionally supports 32-bit widths
 - Supports unbuffered and registered DIMMs

- 2 PCI 2.3 compliant PCI ports, 32 bits each that support 0 to 66 MHz frequencies and on-line insertion and removal
- Local Bus controller providing glueless ROM, Flash, Compact Flash, SRAM, external USB 2.0 devices, and Variable-Latency I/O (VLIO) support with 6 independent chip selects
- 2 Ethernet MAC or Generic Packet Interfaces (GE Subsystem + Generic Device Interface XDMA Controller):
 - Ethernet MAC interfaces support industry-standard TBI (1000 Mbit/s), GMII (1000 Mbit/s), and MII (10/100 Mbit/s, full and half duplex) interface modes
 - Integrated DMA support for GE subsystem:
 - Up to 16 logical channels for each receive and transmit direction (receive and transmit are independent)
 - Supports transmit rate limiter to shape egress traffic on a per-logical channel basis (transmit rate can be limited from 1 Gbits/s full bandwidth down to 64 Kbits/s)
 - Supports simple and weighted round robin for the 16 ingress queues
 - 16 programmable exact address match filters for frames based on Destination or Source Addresses or 802.1Q Tag comparison
 - Programmable all multicast and broadcast frame filtering.
 - Group Multicast address filter via a 256-bin hash lookup table
 - 32-Kbyte scalable packet FIFO with 24 Kbytes for the receive direction, configurable sizing, and support for Ethernet pause flow control
- 2 integrated 16550 UART ports
- 32 Kbytes of on-chip memory (ECC)
- 64 general-purpose I/O pins with integrated de-bounce on 8 pins
- Integrated watchdog timer and 4 general-purpose timers
- Up to 4 ports of Two-Wire interface (TWI) with support for Small Form Factor Plug-able (SFP) or up to 4 ports of MDIO/MDC interface protocol through the general-purpose I/O pins
- Integrated DMA engine, which supports 4 independently configured and controlled channels
- Support for 256 vectored interrupts:
 - In-band interrupt sources from all on-chip GDI devices
 - Flexible mapping of interrupt vectors to E9000 CPU interrupt lines
- Integrated on-chip EJTAG debug circuitry:
 - A dedicated debug module on the E9000 core
 - Watch exceptions, interrupt and exception debuggers, performance counters, and 64-entry trace buffers
- 896-pin FCBGA package, 31 mm x 31 mm
 - Pin compatible with the MSP8510 product

NETWORKED ATTACHED STORAGE SERVER



SUPPORT

OPERATING SYSTEMS

- Open Source Linux versions 2.4 and 2.6
- VxWorks 5.5 from Wind River
- Neutrino from QNX Software Systems

SECURITY TOOLKIT

- Safenet Quicksec
- OpenSSL

EJTAG EMULATORS

- Wind River
- Corelis

EVALUATION BOARDS

- PMC-Sierra PM2330-KIT reference kit
- ATX form-factor evaluation board

COMPANION CHIPS

- Wide range of companion chips available to interface with the PCI bus

APPLICATIONS

- SMB Network Attached Storage (NAS)
- Mid-range VPN routers, firewall and security appliances
- Low-end/Mid-range Enterprise Switches & Routers
- Storage Networking
- IP storage Security appliances
- Office-in-a-box Gateway
- Control Plane Processing
- Imaging systems: Color Laser Printers/MFPs

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